## REMARKS

This amendment is responsive to the Office Action dated January 8, 2007. Claims 33 – 38 are pending in this application and have been rejected. Reconsideration is respectfully requested in view of the foregoing amendments and following remarks. These remarks follow the order of the outstanding Office Action beginning at page 2 thereof.

### Claim Objections

Claim 38 has been objected to as lacking antecedent basis. In response the word "the" has been changed to "an" in order to provide an initial recitation of the Ag-base layer. Applicant also corrects an error in claim 38, line 18 where "in a Si substrate" has been corrected to "is a Si substrate." Support for this correction can be found in the specification at page 30, line 7.

In addition, Applicant noted that in both claims 33 and 38 that the range of y was inconsistent with the specification. The original specification, at page 18, line 14, correctly states the range for y as being $0 \leq y \leq 1$. There is no new matter. This correction has been made in both claim 33 and claim 38.

### Claim Rejections - 35 USC § 103

Applicant's invention is directed to a problem encountered in the construction of light emitting diodes, namely, silicon on the reflective surface which reduces the amount

of reflection and, hence, the efficiency of the LED. Once Applicant discovered that silicon on the reflective surface was a cause of reduced reflectivity, Applicant then proceed with the use of a diffusion blocking layer (layer 35 in both Figures 7 and 9) which may include nickel or titanium as a major component as set forth in claim 34.

In order to better understand Applicant's claims, Applicant includes herein below claims 33 and 38 as now amended with reference numerals to Applicant's Figures. Claim 33 is directed to Figure 7, and claim 38 is directed to Figure 9. The difference between Figure 7 and Figure 9 is that Figure 9 uses a silver reflective layer (310C) while Figure 7 does not include the silver layer. Figure 7 uses a gold reflective layer (310). In either case, the claims (33 and 38) state that the substrate is silicon and that the diffusion barrier blocks diffusion of any device-substrate derived components (particularly Si itself) towards the main layer. This can only mean silicon amongst other components.

Claim 33 and Figure 7

Claim 33 reads on Figure 7 as follows:

33. The light-emitting device comprising:

a compound semiconductor layer having a light-emitting layer portion, being configured so that a first main surface of which serves as a light extraction surface;

wherein the light-emitting layer portion is configured as having a double heterostructure in which a first-conductivity-type cladding layer, an active layer and a second-conductivity-type cladding layer, all of these layers being composed of ($Al_xGa_{1-}$

$_x)_yIn_{1-y}P$ (where, $0 \leq x \leq 1$ and $0 \leq y \leq 1$), are stacked in this order; and

a device substrate **7** bonded on a second main surface side **4** of the compound semiconductor layer while placing a main metal layer **310** in between, the main metal layer **310** having a reflective surface **310a** for reflecting light from the light-emitting layer portion back towards the light extraction surface side **6**; further comprising:

a diffusion-blocking layer **(Ni on layer 31)** interposed between the device substrate and the main metal layer **310**, being composed of a conductive material **Ni**, and provided for blocking diffusion of any device-substrate-derived components towards the main metal layer;

further comprising a substrate-side contact metal layer **31** interposed between the diffusion-blocking layer **35** and the device substrate **7**, intended for reducing contact resistance between the device substrate **7** and the diffusion-blocking layer **35**; and

wherein the main metal layer **310** is composed of an Au-base layer having Au as a major component, at least in a portion including the interface **310, 35** with the diffusion-blocking layer **35**, and the device substrate is a Si substrate.

Claim 38 and Figure 9

Claim 38 reads on Figure 9 as follows:

38. (currently amended) A light-emitting device comprising:

a compound semiconductor layer having a light-emitting layer portion, being configured so that a first main surface of which serves as a light extraction surface;

wherein the light-emitting layer portion is configured as having a double heterostructure in which a first-conductivity-type cladding layer, an active layer and a second-conductivity-type cladding layer, all of these layers being composed of $(Al_xGa_{1-x})_yIn_{1-y}P$ (where, $0 \leq x \leq 1$ and $0 \leq y \leq 1$), are stacked in this order; and

a device substrate **Si** bonded on a second main surface side of the compound semiconductor layer while placing a main metal layer **310** in between, the main metal layer having a reflective surface **310c** for reflecting light from the light-emitting layer portion back towards the light extraction surface side; further comprising;

a diffusion-blocking **35 on** layer **(Ni on layer 31)** interposed between the device substrate **7, Si** and the main metal layer **310**, being composed of a conductive material and provided for blocking diffusion of any device-substrate-derived components **Si** towards the main metal layer **310**;

wherein, the main metal layer **310** is composed of an Au-base, composed of pure Au, or an Au alloy having a ratio of Au content ratio of 95% by mass or above, at least in a portion including the interface with the diffusion-blocking layer **35**, and the device substrate is a Si substrate **7**; and

wherein an Ag-base layer **310c, page 91, line 3** interposed between the Au-base **310 page 86, line 6** layer and the compound semiconductor layer **6, 20**, and having Ag as a major component, composes the reflective layer **310c**.

<u>The Rejection Fails to Meet all Elements</u>

In claim 33, lines 6 – 4 up from the bottom, Applicant claims a substrate-side

contact metal layer interposed between the diffusion blocking layer and the device substrate, intended for reducing contact resistance between the device substrate and the diffusion blocking layer.

This element of claim 33 has not bee discussed in the outstanding Office Action and is not found in any of the references of record. Still further, this element is not suggested by the references of record when taken in combination as will be discussed below.

In the combination of Yasutomi , Carter-Coman, Burt, Gee, and Murasato

Below is a chart showing the teachings of each reference.

| Reference | LED | Si | Reflection | Diffusion Block |
|---|---|---|---|---|
| Yasutomi | Yes | Yes<br>Figure 2,<br>Layer 2 | 3Au | No |
| Carter-Coman | Yes | No Si at all<br>(solder) | 34Ag | 3 blocks solder layer |
| Burt | No | Yes<br>38 | NO | 98 steps to propose conductivity |
| Gee | Yes | No<br>$Al_2O_3$<br>sapphire | 20<br>contact | $Al_2O_3$ diffusion block to prevent oxidation<br><br>Not Si on Au |
| Murasato | No | No | DBR (Bragg reflection layer)<br>No Si Contamination issue | No |
| | | | | |

In the above chart, Applicant lays out all five references relied upon by the Examiner. Yasutomi, as noted by the Examiner, is an LED device having a silicon substrate (Figure 2, layer 2), a gold reflector (3). However, as the Examiner correctly notes, there is no suggestion in Yasutomi of a diffusion block to prevent silicon contamination of the gold layer and, hence, reduction of the reflective capability of the gold layer and, therefore, degradation of the efficiency of the device.

Carter-Coman is an LED device, but contains no silicon. Carter-Coman has a silver reflective layer. Carter-Coman teaches that the solder layer should be blocked from contaminating of the silver layer. This does not suggest blocking of the silicon and other components from the substrate from contamination of the reflective layer.

Burt is not an LED device and has no reflector. Instead, Burt is a semiconductor chip mounting system. In Burt, there is silicon (38). In Burt layer (98) NiV stops silicon from producing a silicon oxide layer on the surface of the gold (40) (see column 6, line 44). The purpose is not at all related to reflectivity because, and as stated in column 6, line 19, it is related to electrical contact resistance. Another reason that the patent does not suggest any effect on reflectivity is that the components are inside and never seen and this is not an LED device. Therefore, there is not suggestion that silicon should be blocked from reaching a reflective layer (gold or silver).

Gee is an LED device, but the substrate is sapphire ($Al_2O_3$). The contacts are gold, therefore, the patent does not suggest that there is any problem with a silicon from the substrate reaching the surface of a reflector (AuAg) which would cause reduced reflectance and, hence, reduced efficiency. It teaches that sapphire has lower

conductivity than silicon (column 2, lines 25 – 30).

Murasato, as the Examiner correctly notes, is an LED device. However, it does not include silicon, it does not have a reflector. Instead, it uses a DBR device (Bragg reflection layer). There is simply no contamination of the reflective layer with respect to a DBR device. Therefore, there is no suggestion that silicon presence in the reflective layer would have any effect upon the efficiency of the device. Absent recognition of the problem of Si on the reflective layer, there is no suggestion of a reason to block silicon and no suggestion of the claimed invention.

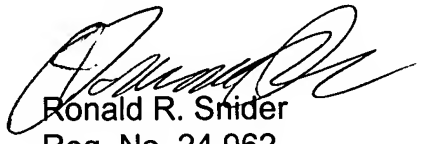
Although the references when taken individually include the elements of Applicant's claims, there is no suggestion that silicon present on the reflective layer would have any effect on the performance of an LED device. The Examiner, in the outstanding Office Action, has given no explanation of any suggestion or reason to combine the references in the manner stated.

Still further, the Examiner has misinterpreted the Carter-Coman reference. Carter-Coman, according to the Examiner, has a contact layer and a silicon-diffusion blocking layer in its teachings. However, Carter-Coman, lacking silicon, cannot teach silicon-diffusion blocking.

In view of the foregoing, it is respectfully submitted that the application is now in condition for allowance, and early action in accordance thereof is requested. In the event there is any reason why the application cannot be allowed in this current

condition, it is respectfully requested that the Examiner contact the undersigned at the number listed below to resolve any problems by Interview or Examiner's Amendment.

Respectfully submitted,



Ronald R. Snider
Reg. No. 24,962

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Snider & Associates
Ronald R. Snider
P.O. Box 27613
Washington, D.C. 20038-7613
Tel.: (202) 347-2600

RRS/bam